ABSTRACT

Methods and apparatus are provided for issuing instructions in a processor having a pipeline. A method includes providing a loop buffer for holding program loop instructions and a register file for holding loop control parameters; in response to decoding of a first loop setup instruction, marking a first entry in the register file as a current entry and writing in the first entry loop control parameters represented in the first loop setup instruction; marking the current entry in the register file as an architectural entry in response to the first loop setup instruction being committed; and sending a loop bottom indicator down the pipeline with a loop bottom instruction.

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